VERITY TECHNOLOGY KOREA
㈜베리티테크놀로지코리아 (www.veritytech.co.kr)
경기도 성남시 분당구 황새울로 200번길 36 동부루트빌딩 1108호
TEL : (02) 2057-8815 FAX : (02) 2057-8810

Allegro Package Designer Agenda

2Day (AM 10:00 ~ PM 17:00)

1Day

- Starting Package Designer Environment Variables
- Exploring the User Interface
- Creating a BGA/Via Pad-stack (Symbol Pin)
- Defining the Cross Section
- Using the BGA Generator
- Autogenerating Die Pins and Signal Names
- Adding a Die from a Text File
- Importing a Netlist File
- Auto assigning Nets : Die to Package

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2 Day

- Moving Die Pins / Creating a New Net
- Setting Extended Constraints
- Creating Power Ring/Wire Profile
- Setting Extended Constraints
- Modifying a Connection
- Routing the Outer Flip-chip Routing
- Running Electrical Rules Check
- Generating a Netlist Report
- Export Output Data

Q & A